REMARKS

Claims 16-29 are pending in the application. Applicant expresses appreciation for the indication that claims 19-21 and 23 set forth allowable subject matter.

Claims 16-18 stand rejected under 35 U.S.C. 102(e) as being anticipated by Al Shareef. Applicant requests reconsideration.

Claim 16 sets forth a capacitor construction that includes, among other features, a surface area enhancement layer over a substrate, a first capacitor electrode over the enhancement layer, a capacitor dielectric layer over the first electrode, and a second capacitor electrode over the dielectric layer. The enhancement layer has an outer surface area per unit area that is greater than an inner surface area per unit area of the enhancement layer. The first electrode has an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. The first electrode does not comprise the enhancement layer. Page 3 of the Office Action alleges that Al-Shareef discloses each and every limitation of claim 16. Applicant traverses on the ground that Al-Shareef fails to disclose an enhancement layer that is not comprised by a first electrode, as set forth in claim 16.

Page 3 of the Office Action alleges that double metal layer 144 of Al-Shareef functions as a first capacitor electrode but does not comprise HSG polysilicon layer 142 as a part of such electrode. Applicant asserts that the Office's interpretation is impossible and prevents the memory cells of Al-Shareef from functioning as intended. As may be understood from column 1, lines 28-31 and column 2, lines 4-23 of Al-Shareef, those of ordinary skill clearly appreciate that any capacitor charge stored by

double metal layer 144 functioning as a capacitor electrode must be electrically connected through HSG polysilicon layer 142 and conductive polysilicon material 134 to the underlying drain regions 106. This electrical connection is shown in Figs. 11-13 and the text associated therewith. Since HSG polysilicon layer 142 is positioned between double metal layer 144 and conductive polysilicon material 134, HSG polysilicon layer 142 must be conductive. Being conductive, HSG polysilicon layer 42 must be comprised by the capacitor electrode of Al-Shareef in order for a capacitor charge of such electrode to be electrically connected to drain regions 106.

As implied at least by page 17, lines 1-6 of the present specification, if HSG polysilicon layer 142 is not conductive and, thus, is not comprised by the Al-Shareef capacitor electrode, then the Al-Shareef memory cell cannot function as intended. Those of ordinary skill clearly understand this basic functional requirement of HSG polysilicon layer 142 that the Office has apparently overlooked. Given the capacitor structure shown in Fig. 13 of Al-Shareef and the text associated therewith, it is impossible for HSG polysilicon layer 142 not to be comprised by the capacitor electrode. Any allegation otherwise contradicts the requirement that the Al-Shareef memory cell function as intended. The Office's interpretation of the properties of HSG polysilicon layer 142 cannot result in frustration of the Al-Shareef memory cell intended function.

Al-Shareef further supports the Applicant's position with its ample discussion in column 5, lines 35-55 of the requirement that barrier metal layer 146 remain conductive even after any subsequent oxidation or degradation of layer 146. Column 2, line 45 to column 3, line 5 of Al-Shareef also discusses reduced conductivity of layers comprised

by capacitor electrodes as a problem in the prior art that Al-Shareef is intended to overcome. The Office's interpretation of Al-Shareef reintroduces a similar problem that Al-Shareef was intended to overcome.

At least for the reasons indicated herein, Applicant asserts that Al-Shareef fails to disclose each and every limitation of claim 16 and does not anticipate claim 16. Claims 17 and 18 depend from claim 16 and are not anticipated at least for such reason as well for the additional limitations of such claims not disclosed. Accordingly, Applicant requests allowance of claims 16-18 in the next Office Action.

Claims 22 and 24-29 stand rejected under 35 U.S.C. 102(b) as being anticipated by Fukuzumi. Applicant requests reconsideration.

Claim 22 sets forth a capacitor construction that includes, among other features, an opening in an insulative layer over a substrate, a hemispherical grain polysilicon layer over the sides of the opening but not over the bottom, a conformal first capacitor electrode on the polysilicon, a capacitor dielectric layer on the first electrode, and a second capacitor electrode over the dielectric layer. The first electrode is sufficiently thin that the first electrode has a rugged outer surface with an outer surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode. Pages 4 and 8 of the Office Action allege that Fukuzumi discloses each and every element of claim 22. However, Applicant asserts that Fukuzumi fails to disclose any single capacitor construction that includes each of the claim limitations.

Page 8 of the Office Action rebuts Applicant's assertion by stating that "Fukuzumi et al disclose clearly each single capacitor construction that includes limitations cited in the claim 22 [sic]," referring to Figs. 18-24 and the text associated therewith.

Nevertheless, thorough review of the relied upon portions of Fukuzumi does not reveal any support for the Office's allegation.

Turning to the sequential capacitor formation process depicted in Figs. 18-24, the Office Action alleges that Fig. 22 discloses lower electrode 24 as the first capacitor electrode of claim 22 and silicon oxide films 23A as the hemispherical grain polysilicon layer of claim 22. Applicant notes that Fig. 22 and the text associated therewith constitute the sole disclosure in Figs. 18-24 of lower electrode 24 being on silicon oxide films 23A. However, Fukuzumi is completely devoid of any disclosure of a capacitor dielectric layer on lower electrode 24 or a second capacitor electrode over the dielectric layer in a capacitor construction that also discloses lower electrode 24 on silicon oxide films 23A. Thus, Fukuzumi fails to disclose each and every limitation of claim 22.

Applicant acknowledges that Fig. 24 and the text associated therewith show high-dielectric film 26 over lower electrodes 24 and upper electrode 27 over high-dielectric film 26. However, Fukuzumi is completely devoid of any disclosure that the structure of Fig. 24 may include silicon oxide films 23A. Accordingly, Fig. 24 also fails to disclose each and every limitation of claim 22.

The Office appears to be of the seriously mistaken view that features of Fig. 22 can be somehow combined with features of Fig. 24 to produce a device anticipating claim 22. However, a finding of anticipation requires disclosure of the modification of Figs. 22 and 24 relied upon. Fukuzumi does not provide any such disclosure and the Office Action does not allege that Fukuzumi provides any such disclosure. Instead, Fukuzumi merely describes complete removal of silicon oxide films 23A from lower electrode 24, as shown in Fig. 23, prior to any formation of high-dielectric film 26 or

upper electrode 27. It is inconceivable that Fukuzumi can somehow be considered to disclose each and every limitation of claim 22 given the deficiencies of such reference.

In the event that the Office becomes inclined to allege that claim 22 is obvious over Fukuzumi based upon some yet-to-be-identified modification of Fukuzumi's disclosure, Applicant asserts that claim 22 remains patentable over Fukuzumi. The test for establishing an implicit teaching, motivation, or suggestion for the combination of two statements within a single prior art reference is to view what such statements would have suggested to those of ordinary skill. In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). The two statements must be considered in the context of the entire reference's teaching and cannot be viewed in the abstract. Id. A rejection cannot be predicated on the mere identification in the reference of individual components of claimed limitations. Id. Instead, particular findings must be made as to the reason a person of skill would, with no knowledge of the claimed invention, select the components of the two statements for combination in the manner claimed. Id.

Applicant asserts that no teaching, motivation, or suggestion exists or is alleged by the Office to exist somehow to combine the features of Fig. 22 and Fig. 24 to produce the capacitor construction of claim 22. Further, Applicant asserts that including silicon oxide films 23A of Fig. 22 with the structure shown in Fig. 24 would frustrate the intended purpose set forth in Fukuzumi of removing silicon oxide films 23A to obtain structural advantages described by Fukuzumi for the Fig. 24 structure.

Claims 24-26 depend from claim 22 and are not anticipated at least for such reason as well as for the additional limitations of such claims not disclosed. Applicant further asserts that claims 24-26 are patentable over Fukuzumi.

Claim 27 sets forth a capacitor construction that includes, among other features, a surface area enhancement layer containing undoped polysilicon over a substrate, a first capacitor electrode on and in direct contact with the enhancement layer, a capacitor dielectric layer over the first electrode, and a second capacitor electrode over the dielectric layer. The enhancement layer has an outer surface are per unit area that is greater than an inner surface area per unit area of the enhancement layer. The first capacitor electrode does not contain the enhancement layer as part of the first electrode. Also, the first electrode has an inner surface are per unit area and an outer surface area per unit area that are both greater than the inner surface area per unit area of the enhancement layer. Pages 5 and 8 of the Office Action allege that Fukuzumi discloses every limitation of claim 27. However, Applicant asserts that Fukuzumi fails to disclose an enhancement layer containing undoped rugged polysilicon. Fukuzumi also fails to disclose a first capacitor electrode that does not include the enhancement layer as part of the first electrode.

Page 8 of the Office Action rebuts the Applicant's assertion by stating that column 7, lines 24-36 of Fukuzumi disclose practicing the Fukuzumi method by "other HSG technologies." Applicant asserts that such allegation by the Office is irrelevant because the interpretation of Fukuzumi alleged by the Office is impossible and prevents the memory cell containing the Fukuzumi capacitor structures from functioning as intended.

Claim 27 expressly states that the first capacitor electrode does not comprise the surface area enhancement layer as part of the first electrode. Page 5 of the Office Action alleges that polysilicon film 51 discloses the claimed surface area enhancement

layer. However, column 14, lines 62-65 of Fukuzumi expressly state that "polysilicon film 51 forms part of the lower electrode of a capacitor." Thus, the Office's allegation contradicts the express teachings of Fukuzumi. The surface area enhancement layer of claim 27 is not comprised by the claimed first capacitor electrode. This claim limitation is in opposition to the express requirement in Fukuzumi that polysilicon film 51 forms a part of the lower electrode of a capacitor. Nowhere does the Office Action provide any mention of the claim 27 limitation that the first capacitor electrode does not comprise the enhancement layer.

The Applicant previously asserted such failing of Fukuzumi on multiple occasions and, yet, the Office Action persists in failing to provide any basis by which Fukuzumi can be considered to disclose such limitation of claim 27. At least for such reason, Fukuzumi fails to disclose or suggest every limitation of claim 27.

Column 14, lines 62-65 of Fukuzumi expressly state that "polysilicon film 51 forms part of the lower electrode of a capacitor." In this manner, polysilicon film 51 provides electrical connection for capacitor charge between metal film 52 of the capacitor electrode and contact plug 3. Contact plug 3 is, in turn, electrically connected to a memory cell transistor, as discussed in the Abstract and throughout Fukuzumi. The required function of polysilicon film 51 as part of a capacitor electrode precludes such material from including undoped rugged polysilicon, as set forth in claim 27. Pages 5 and 8 of the Office Action allege that it is inherent in Fukuzumi that polysilicon film 51 may be undoped rugged polysilicon. However, such a composition would frustrate the intended purpose of polysilicon film 51 to function as an electrical connection between metal film 52 and contact plug 3.

In relying upon the theory of inherency, the Office must provide a basis in fact and/or technical reasoning to support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the relied upon reference. Applicant asserts that it is inconceivable for polysilicon film 51 inherently to comprise undoped rugged polysilicon since such allegedly inherent characteristic cannot be considered to flow from the teachings of Fukuzumi. Instead, Fukuzumi precludes such an inherent teaching as frustrating the intended purpose of polysilicon film 51. At least for such additional reason, Fukuzumi fails to disclose every limitation of claim 27 and does not anticipate claim 27.

Claim 28 sets forth a capacitor construction that includes, among other features, an opening having sides and a bottom in an insulative layer, a HSG polysilicon layer over the sides of the opening but not over the bottom, a conformal first capacitor electrode on the HSG polysilicon layer, a capacitor dielectric layer on the first electrode, and a second capacitor electrode over the dielectric layer. The first capacitor electrode does not include the HSG polysilicon layer as part of the first electrode. Also, the first electrode is sufficiently thin that the first electrode has a rugged outer surface with an outer surface area per unit area greater than a surface area per unit area of the sides of the opening over which the HSG polysilicon layer is formed. Pages 5-6 and 9 of the Office Action allege that Fukuzumi discloses every limitation of claim 28. However, Applicant asserts that Fukuzumi fails to disclose any single capacitor construction that includes all of the limitations set forth in claim 28.

As may be appreciated from the above discussion regarding the deficiencies of Fukuzumi as applied to claim 22, Fukuzumi fails to disclose each and every limitation of claim 28. At least for such reason, Fukuzumi fails to anticipate claim 28.

In addition, claim 28 sets forth that the first capacitor electrode does not comprise the HSG polysilicon layer as part of the first electrode. Page 9 of the Office Action refers to Fig. 4 of Fukuzumi as allegedly disclosing the claimed first capacitor electrode on the HSG polysilicon layer but not including the HSG polysilicon layer as part of the first electrode. Nevertheless, it is irrelevant whether or not Fig. 4 discloses such a structure because Fig. 4 fails to disclose a capacitor dielectric layer on the first electrode and a second capacitor electrode over the dielectric layer. Accordingly, Fukuzumi still fails to provide any disclosure of a capacitor construction that includes every limitation of claim 28. At least for such additional reason, Fukuzumi does not anticipate claim 28. Claim 29 depends from claim 28 and is not anticipated at least for such reason as well as for the additional limitations of such claim not disclosed.

As apparent from the discussion above, Fukuzumi does not anticipate claims 22 and 24-29 and Applicant requests allowance of such claims in the next Office Action.

Applicant herein establishes adequate reasons supporting patentability of claims 16-29 and requests allowance of all such pending claims in the next Office Action.

Respectfully submitted,

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James E. Lake
Reg. No. 44,854